ADCMOS Practical’s with 90nm Technology

**Tool:**  NGSPICE

**Practical – 1**

**Aim:** Plot characteristic curves of NMOS, PMOS, plot DC load line and calculate channel length modulation factor (lambda), sub threshold slop, sub threshold current, gm, gds, gm/gds,

* + 1. Plot of Id vs Vgs at different drain voltages for NMOS, PMOS.
    2. Plot of Id vs Vgs at particular drain voltage (low) for NMOS, PMOS and Finding Vt.
    3. Plot of log Id vs Vgs at particular gate voltage (high) for NMOS, PMOS and determine Ioff and Sub threshold slope.
    4. Plot of Id vs Vds at different gate voltages for NMOS, PMOS and Finding Channel length modulation factor.

**Program:**

1(a). ID vs VGS at different drain voltages for NMOS.

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

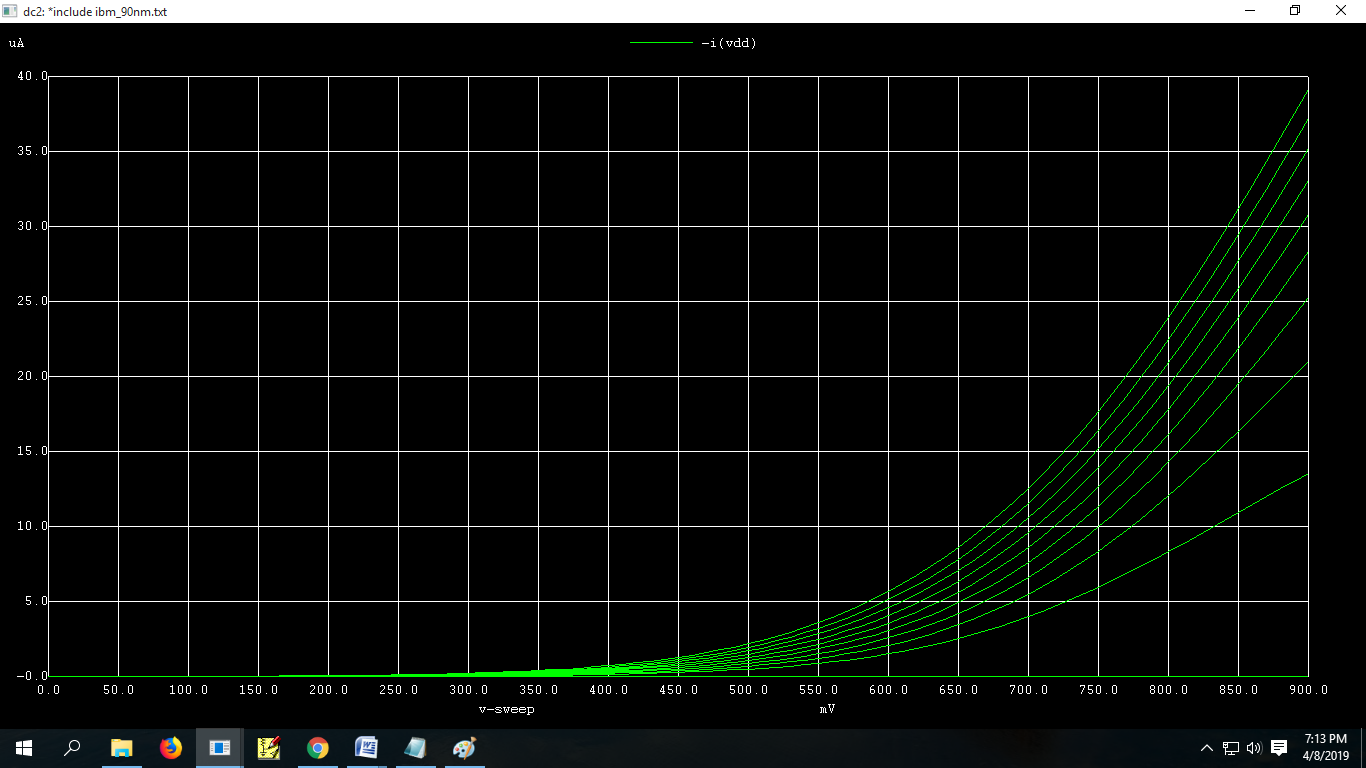
dc vgs -2 2 10m vdd 0 0.9 0.1

plot -i(Vdd)

.endc

.end

**SCREENSHOTS:**



1(b). ID vs VGS at different drain voltages for PMOS

.include ibm\_90nm.txt

vds 0 2 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

run

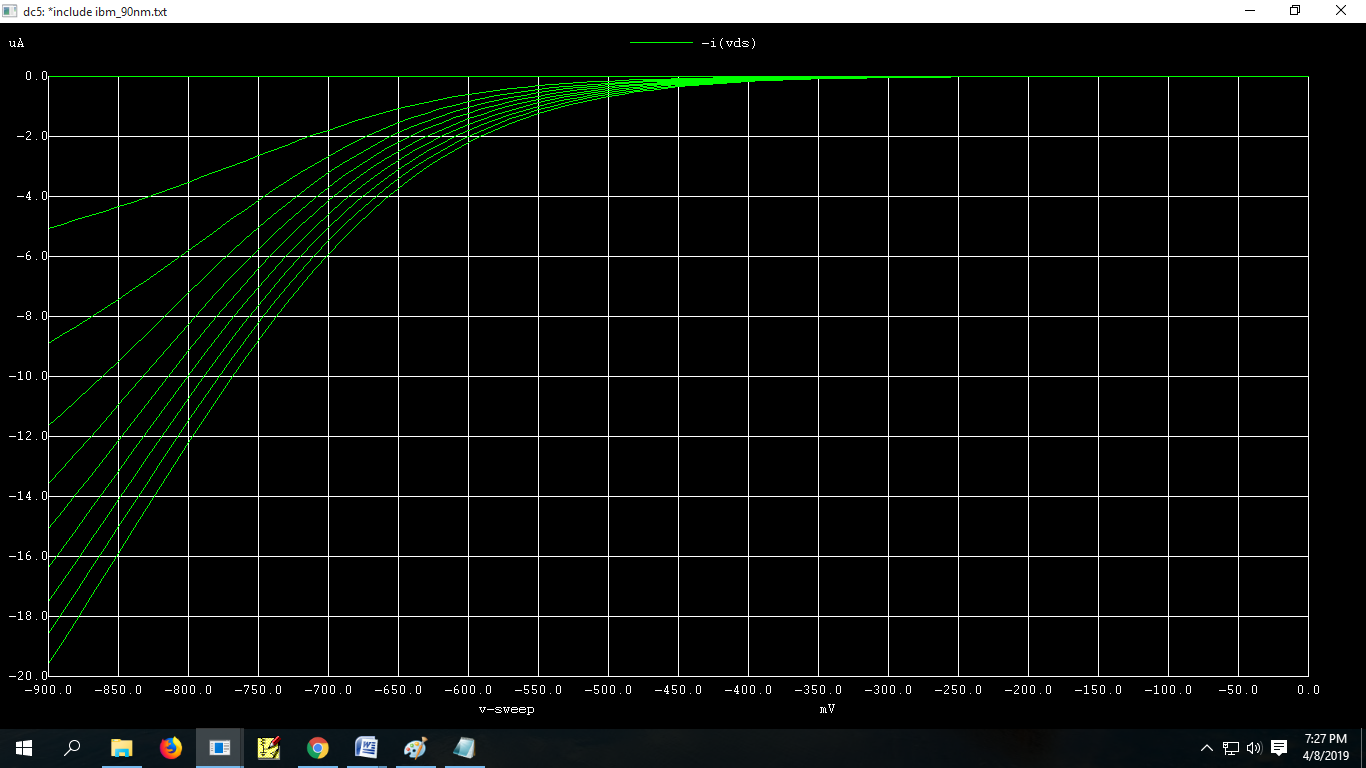
dc vgs 0 -0.9 -0.01 vds 0 -0.9 -0.1

plot -i(vds)

.endc

.end

**SCREENSHOTS:**



2(a). Id vs Vgs at particular drain voltage (Vds =0.45v) for NMOS and finding Vt.

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

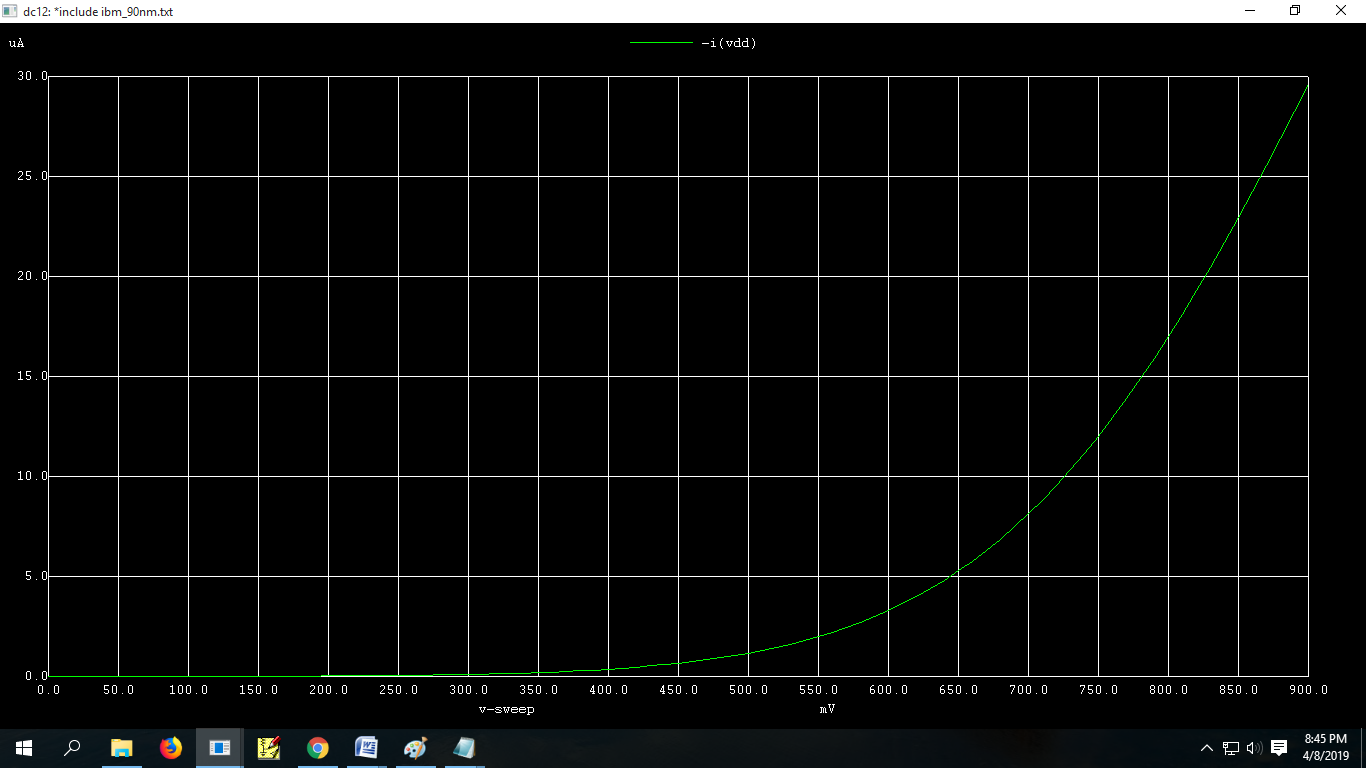
dc vgs 0 0.9 10m vdd 0.45

plot -i(Vdd)

.endc

.end

**SCREENSHOTS:**

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**Conclusion:** Vth of nmos for (Vds=0.45 ) is 0.35v

2(b). Id vs Vgs at particular drain voltage (Vds =-0.45v) for PMOS and finding Vt.

.include ibm\_90nm.txt

vds 0 2 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

run

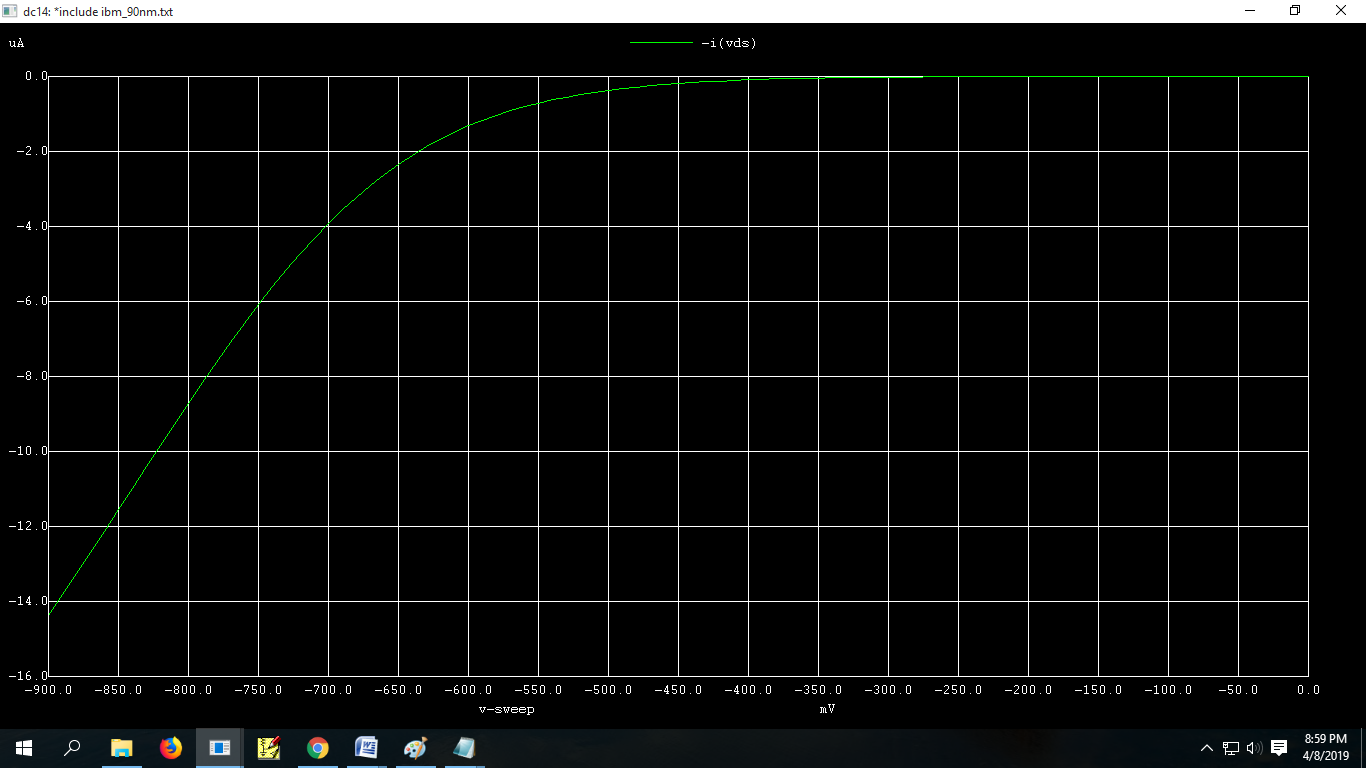
dc vgs 0 -0.9 -0.01 vds -0.45

plot -i(vds)

.endc

.end

**SCREENSHOTS:**

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**Conclusion:** Vth of pmos for (Vds=-0.45 ) is -0.4v

3(a). log Id vs Vgs at particular gate voltage (high) for NMOS and Finding Ioff and Subthreshold slope

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

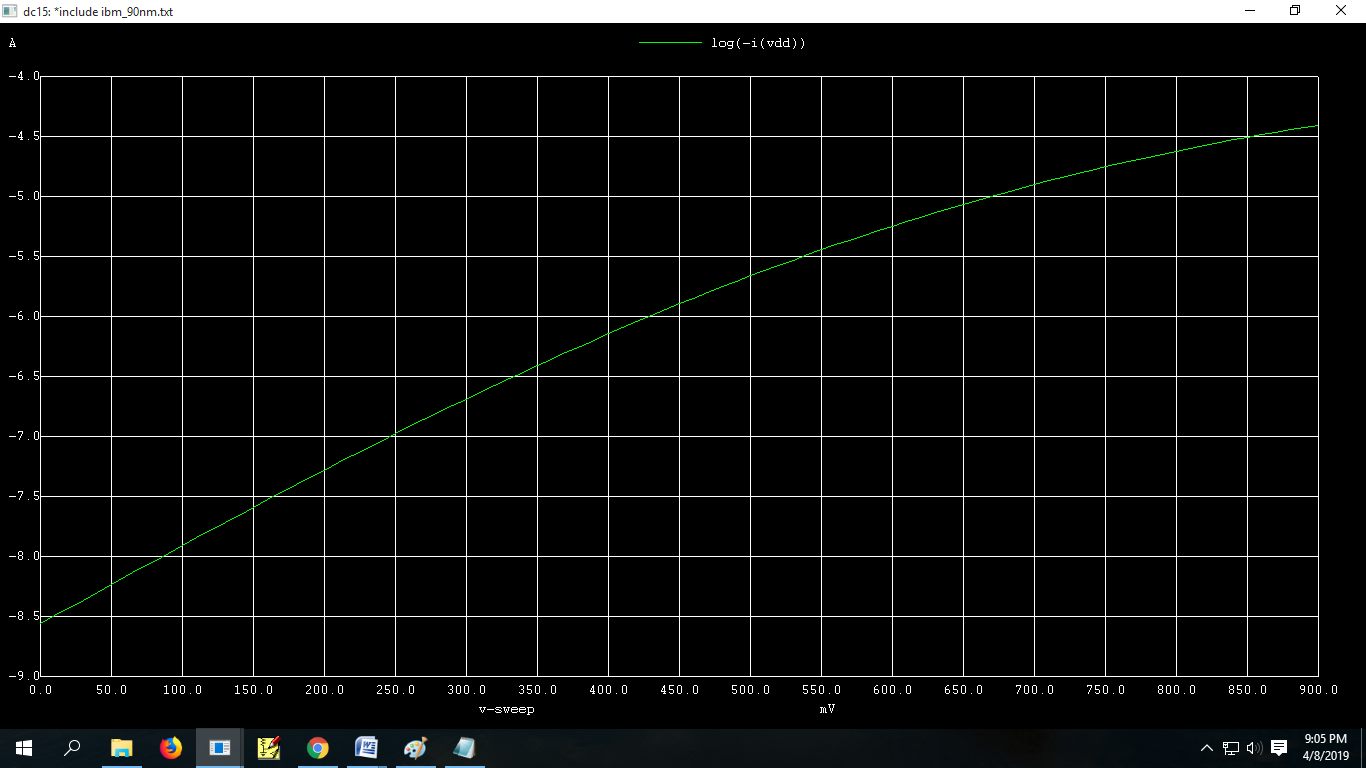
dc vgs 0 0.9 0.01

plot log(-i(Vdd))

.endc

.end

**SCREENSHOTS:**

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**Conclusion:** Sub threshold current is and sub threshold slop is 174m.

3(b). log Id vs Vgs at particular gate voltage (high) for PMOS and Finding Ioff and Subthreshold slope

.include ibm\_90nm.txt

vdd 0 2 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

run

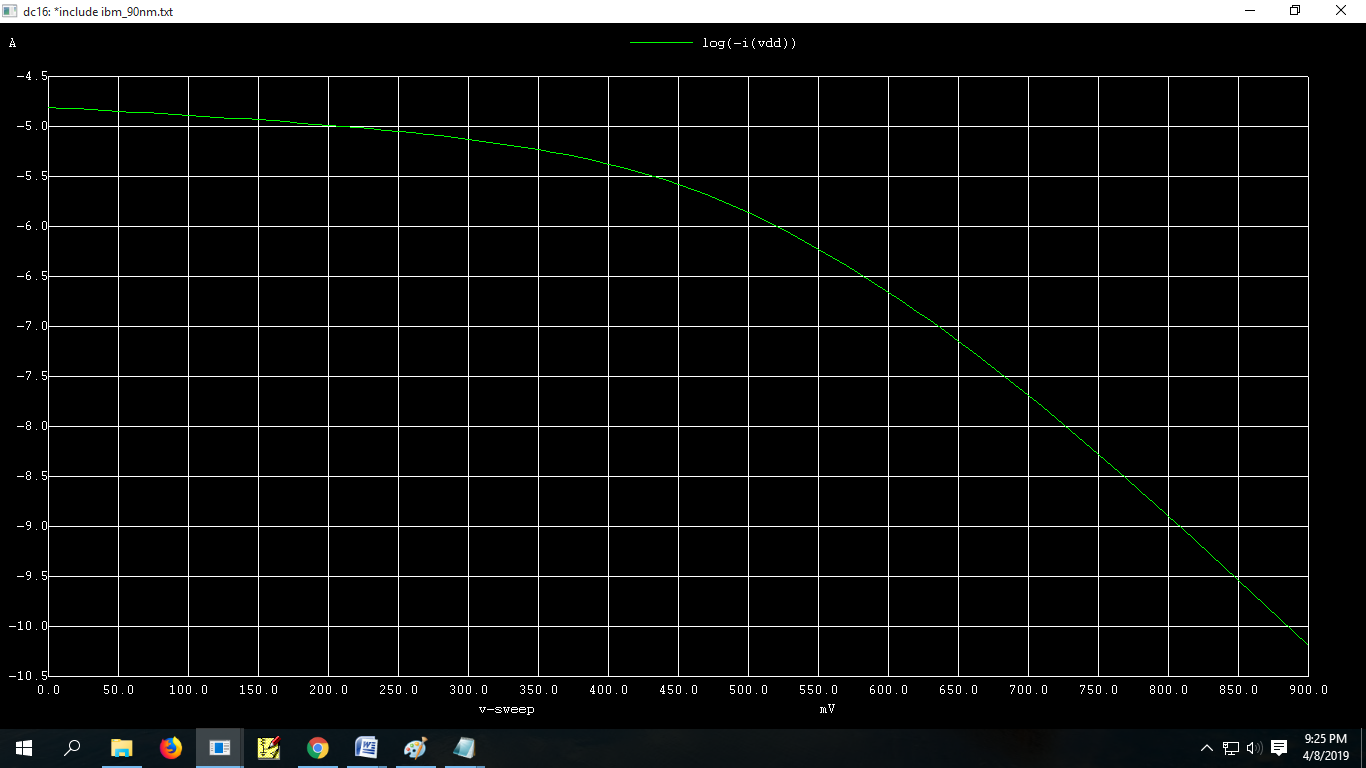
dc vgs 0 0.9 0.01

plot log(-i(Vdd))

.endc

.end

**SCREENSHOTS:**

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**Conclusion:** Sub threshold current is and sub threshold slop is 79m

4(a) Id vs Vds at different gate voltages for NMOS and finding Channel length modulation factor (lambda)

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

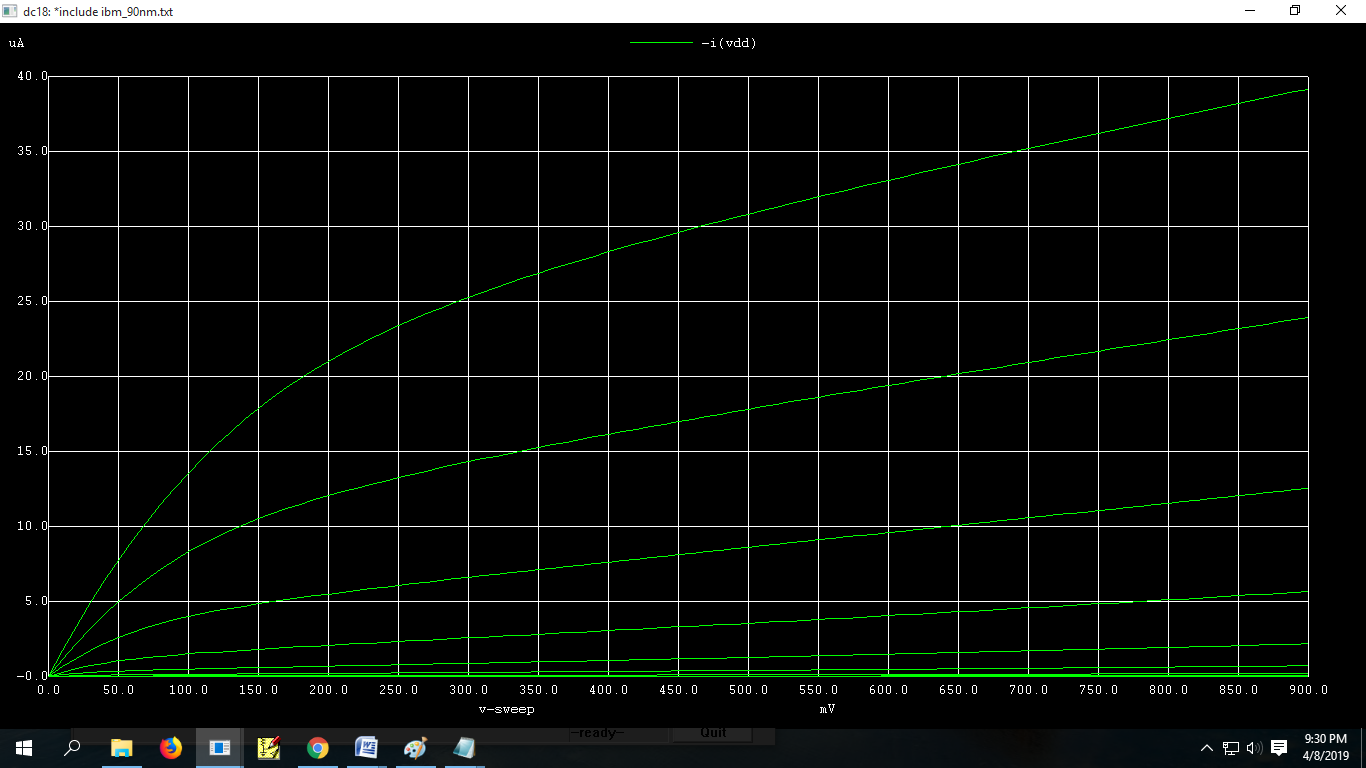
dc vdd 0 0.9 10m vgs 0 0.9 0.1

plot -i(Vdd)

.endc

.end

**SCREENSHOTS:**

****

**Conclusion:** Channel length modulation factor (lambda) =0.542

4(b). Id vs Vds at different gate voltages for NMOS and finding Channel length modulation factor (lambda)

.include ibm\_90nm.txt

vds 0 2 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

run

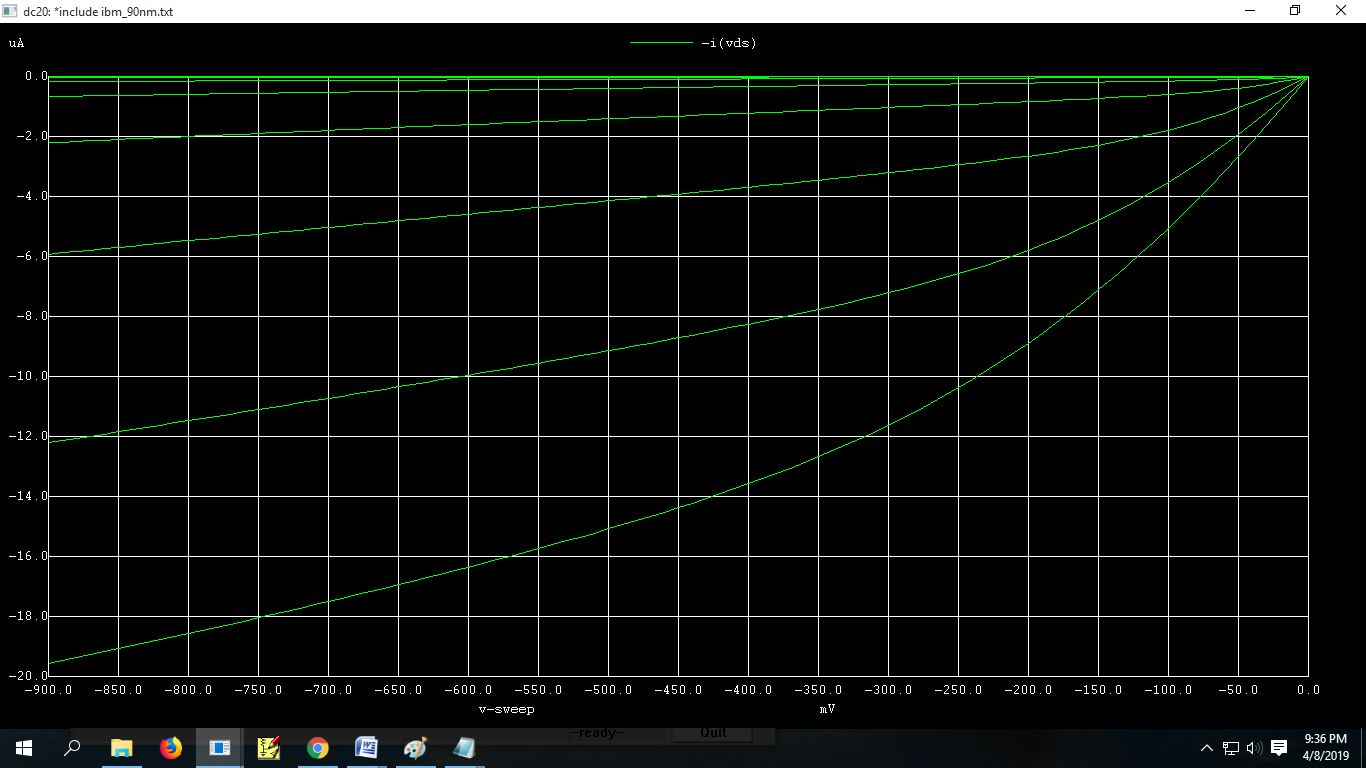
dc vds 0 -0.9 -10m vgs 0 -0.9 -0.1

plot -i(vds)

.endc

.end

**SCREENSHOTS:**



**Conclusion:** Channel length modulation factor (lambda) =-0.802

In above graph id quadratically depends on vgs i.e, graphs are not equidistance from each other.

**Practical – 2**

**Aim:** 2(a). Extract Vth of NMOS transistors (short channel and long channel).

To extract Vth use the following procedure.

a- Plot gm vs. VGS using NGSPICE and obtain peak gm point.

b- Plot y=ID/(gm)1/2 as a function of VGS using NGSPICE.

c- Use NGSPICE to plot tangent line passing through peak gm point in y(VGS) plane and determine Vth.

There are four methods to find Vth:

1. Linear Region.
2. Ghibaudo Method.
3. Saturation Region.
4. Derivative Method
5. Linear Region:

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

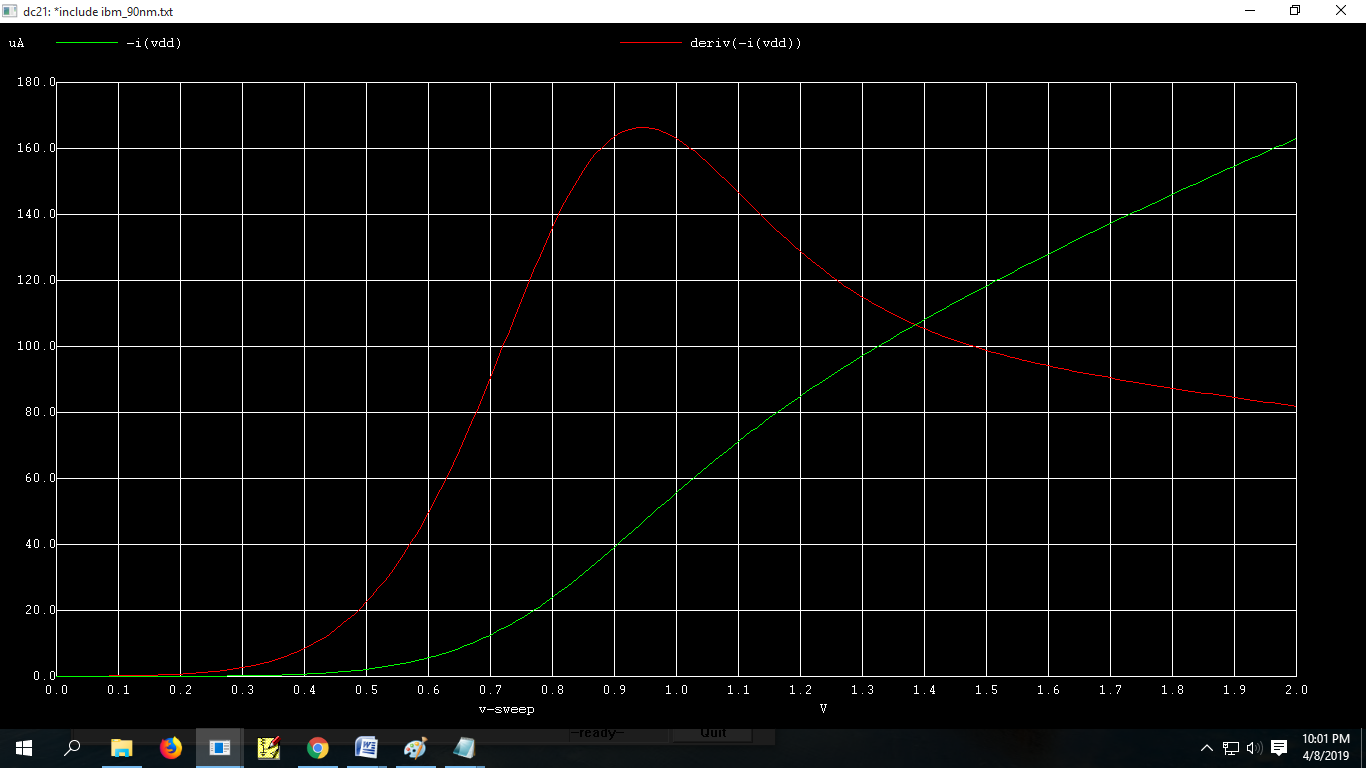
dc vgs 0 2 10m

plot -i(Vdd) deriv(-i(Vdd))

.endc

.end

**SCREENSHOTS**



1. Ghibaudo Method.

.include ibm\_90nm.txt

vdd 2 0 1.8

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

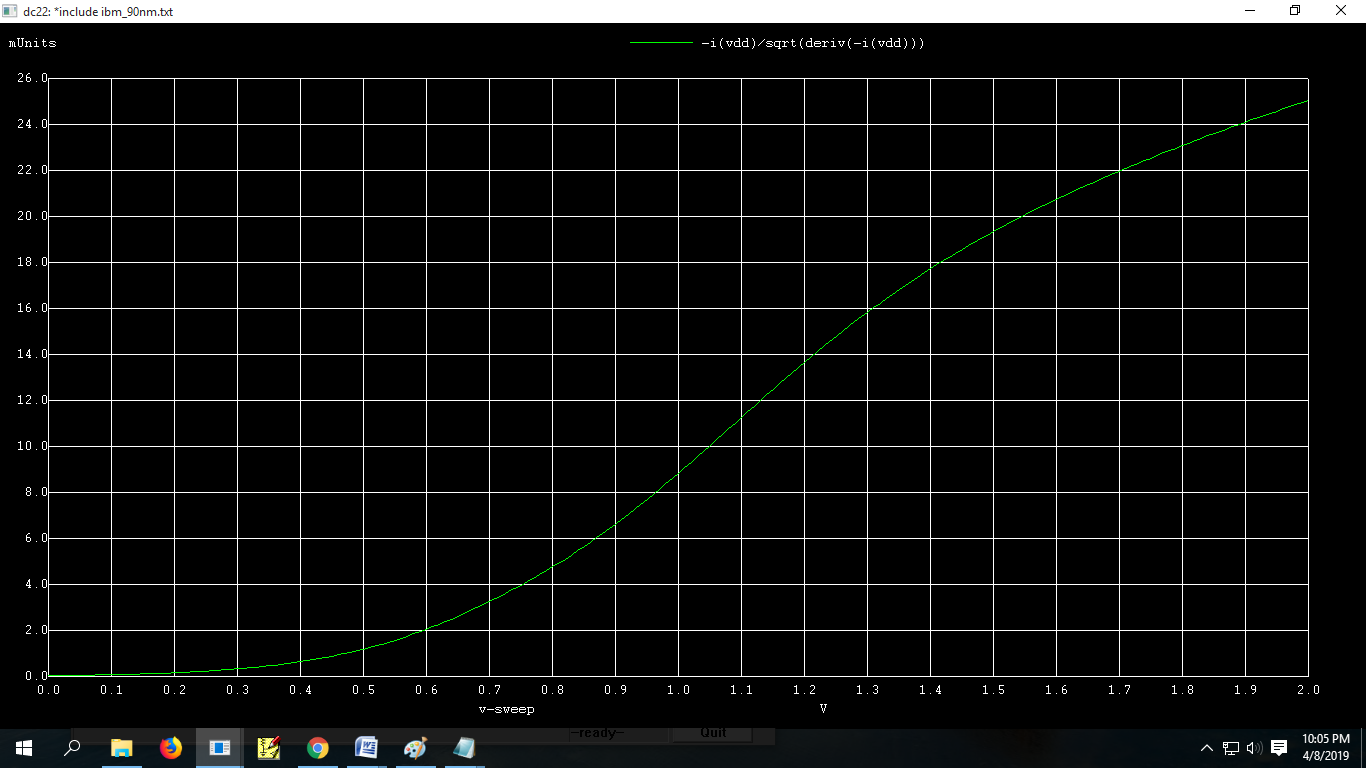
dc vgs 0 2 10m

plot -i(Vdd)/sqrt(deriv(-i(Vdd)))

.endc

.end

**SCREENSHOTS:**



1. Saturation region

.include ibm\_90nm.txt

vdd 2 0 1.8

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

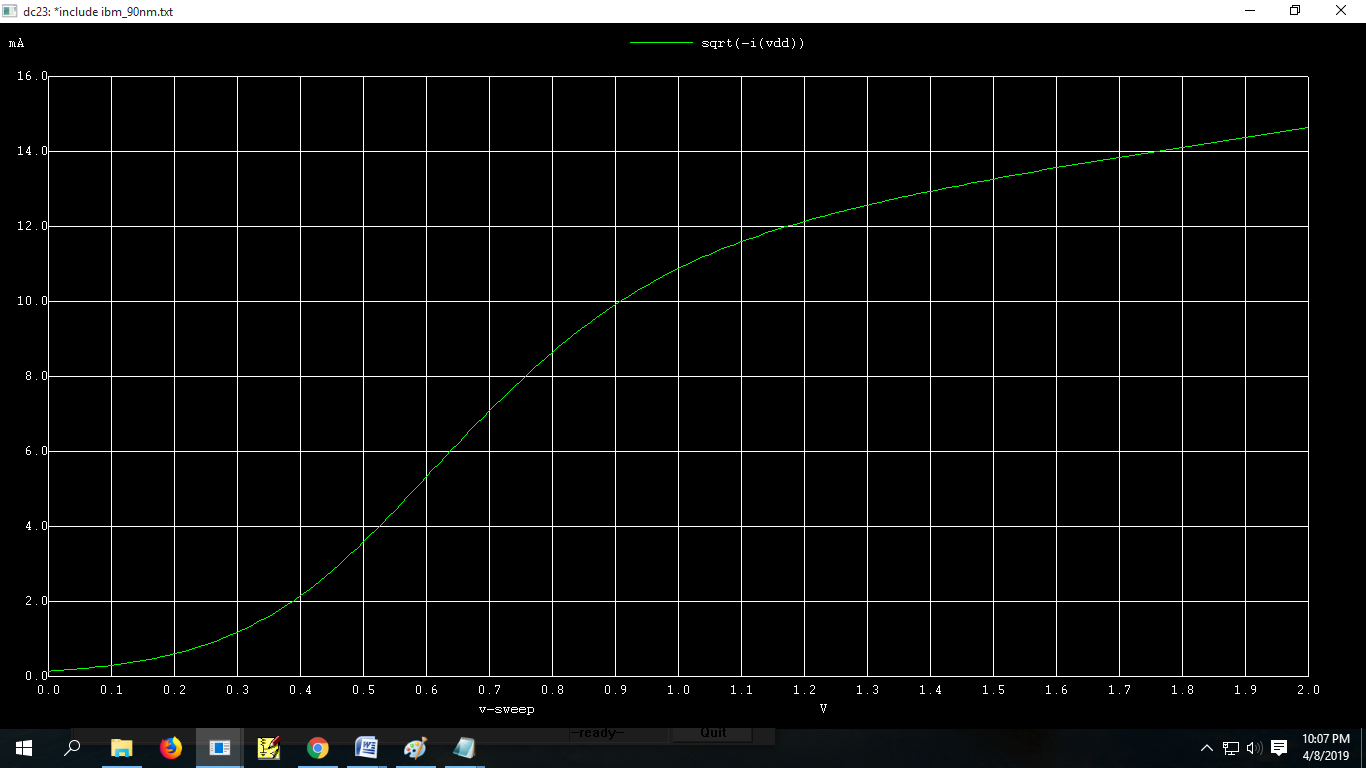
dc vgs 0 2 10m

plot sqrt(-i(Vdd))

.endc

.end

**SCREENSHOTS:**

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1. Derivation Method:

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 0 0.9

MN 2 1 0 0 cmosn l=90n w=180n

.control

run

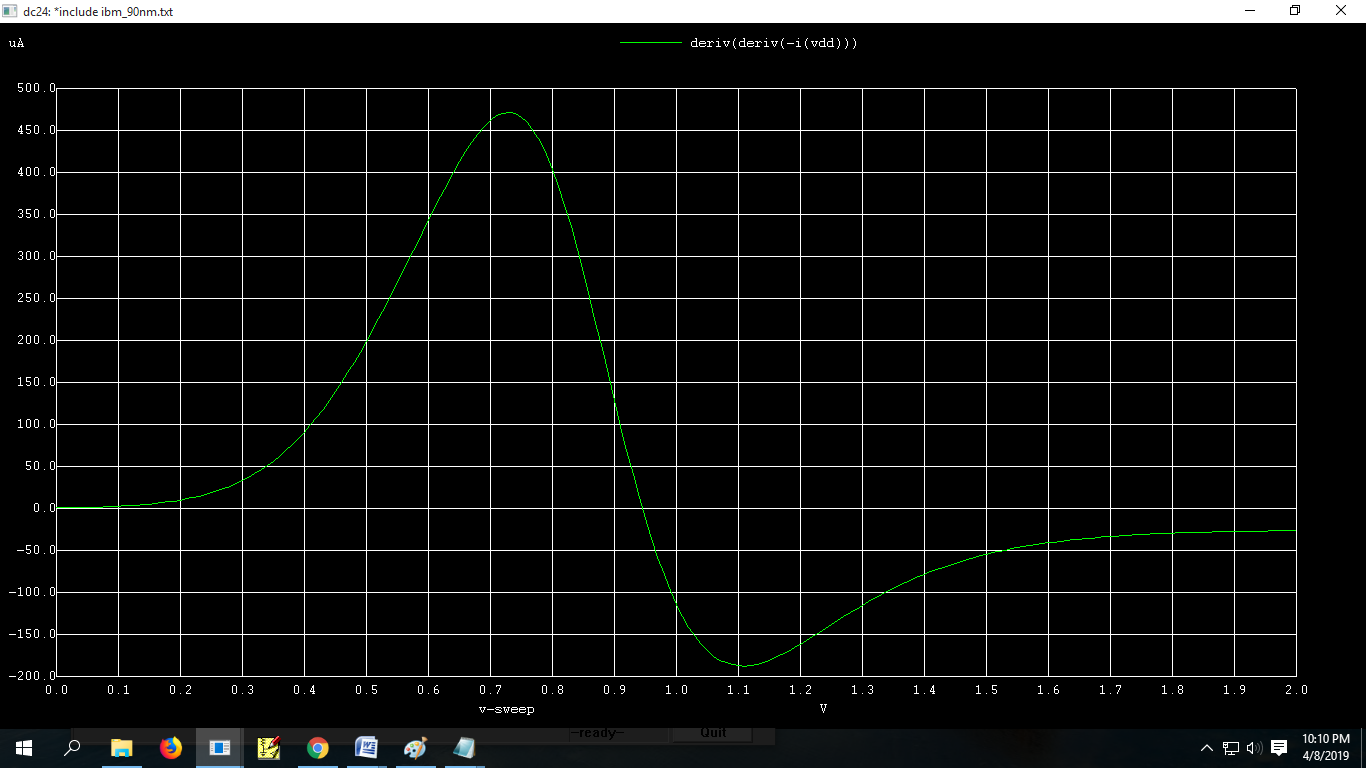
dc vgs 0 2 10m

plot deriv(deriv(-i(Vdd)))

.endc

.end

**SCREENSHOTS:**

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**Conclusion:**  Vth of NMOS by Following Methods

1. Linear Region. = 0.62
2. Ghibaudo Method. = 0.61
3. Saturation Region. = 0.38
4. Derivative Method. = 0.72

2(b) Extract Vth of PMOS transistors (short channel and long channel).

To extract Vth use the following procedure.

a- Plot gm vs. VGS using NGSPICE and obtain peak gm point.

b- Plot y=ID/(gm)1/2 as a function of VGS using NGSPICE.

c- Use NGSPICE to plot tangent line passing through peak gm point in y(VGS) plane and determine Vth.

There are four methods to find Vth:

1. Linear Region.
2. Ghibaudo Method.
3. Saturation Region.
4. Derivative Method
5. Linear Region:

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

run

dc vgs -2 0 10m

plot i(Vdd) deriv(-i(Vdd))

.endc

.end

**SCREENSHOTS**



1. Ghibaudo Method.

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

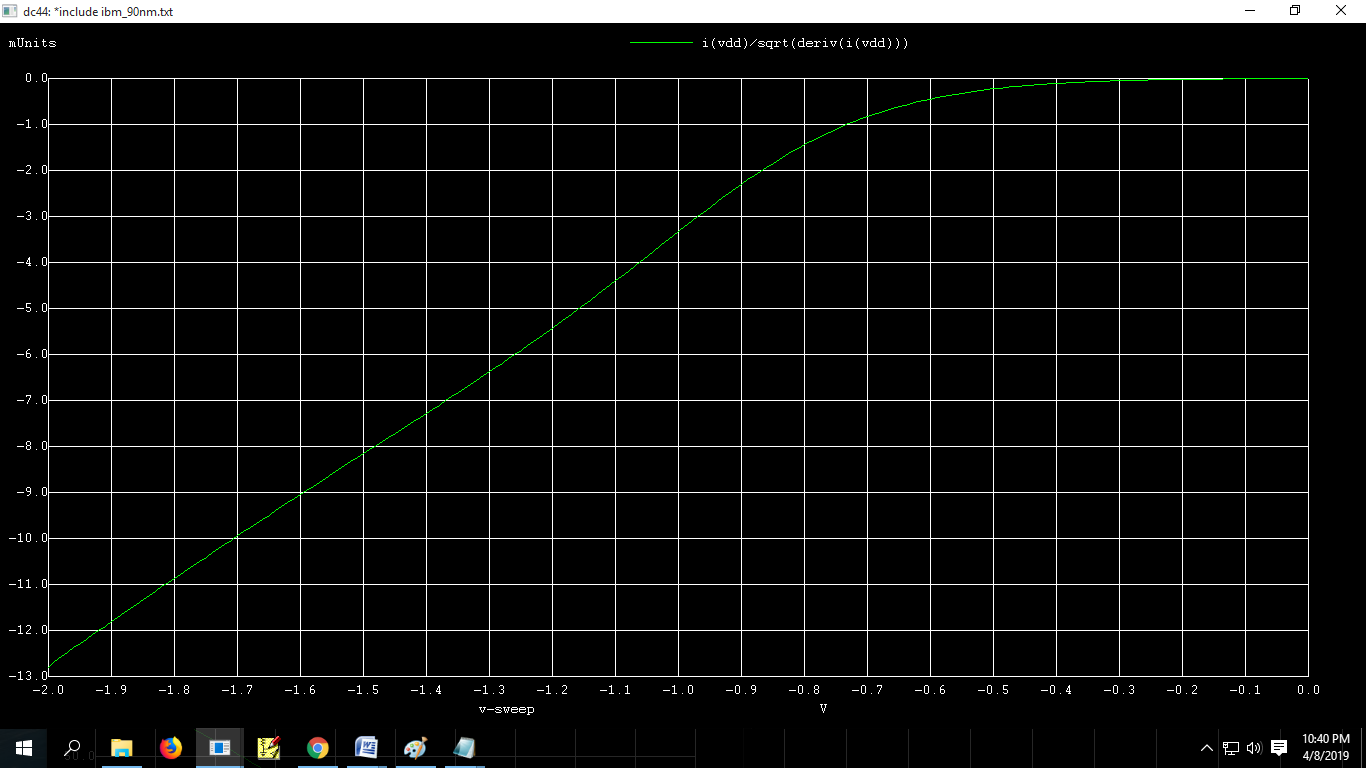
run

dc vgs -2 0 10m

plot i(Vdd)/sqrt(deriv(i(Vdd)))

.end

**SCREENSHOTS:**



1. Saturation region

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

run

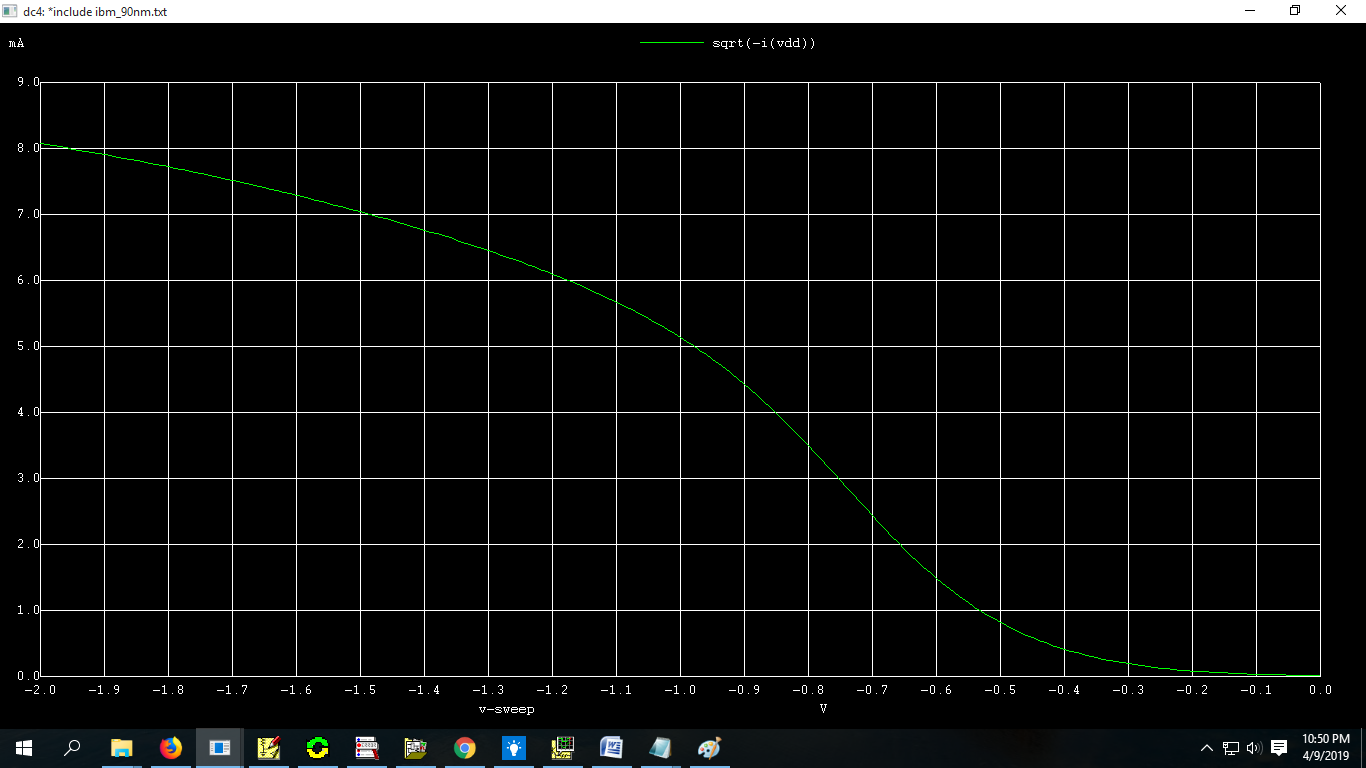
dc vgs -2 0 10m

plot sqrt(-i(Vdd))

.endc

.end

**SCREENSHOTS:**

****

1. Derivation Method:

.include ibm\_90nm.txt

vdd 2 0 0.9

vgs 1 2 0.9

MN 0 1 2 2 cmosp l=90n w=180n

.control

run

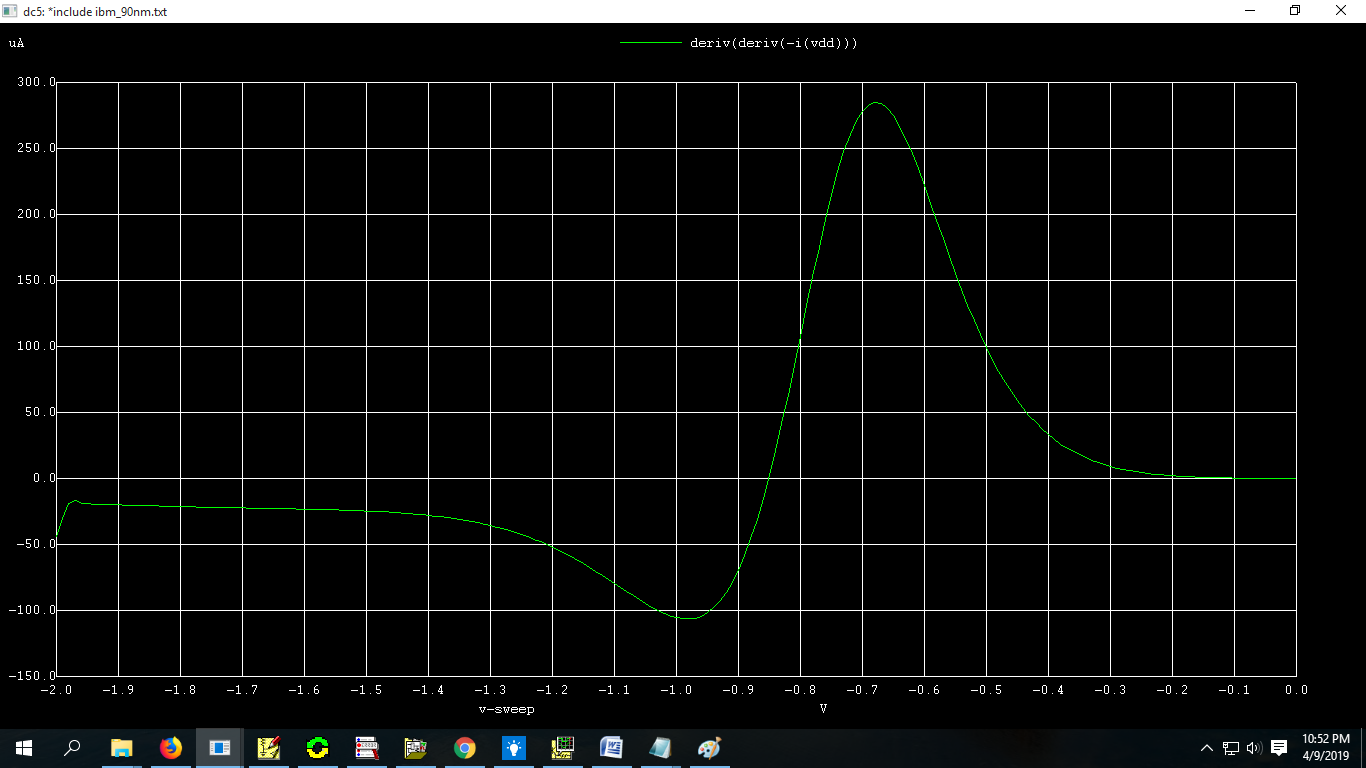
dc vgs -2 0 10m

plot deriv(deriv(-i(Vdd)))

.endc

.end

**SCREENSHOTS:**

****

**Conclusion:**  Vth of PMOS by Following Methods

1. Linear Region. = -0.62
2. Ghibaudo Method. = -0.67
3. Saturation Region. = -0.47
4. Derivative Method. = - 0.675

**Practical – 3**

**Aim:** CMOS Inverter Study

1. Plot VTC curve for CMOS inverter and thereon plot dVout vs dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter. (for formulae refer page 189- Rabaey)
2. Plot VTC for CMOS inverter with varying VDD.
3. Plot VTC for CMOS inverter with varying device ratio.
4. Give pulse to inverter and find tphl , tplh, td.
5. VTC curve of Inverter

.include ibm\_90nm.txt

vdd 2 0 0.9

vin 1 0 0.9

vref 4 0 -1

mn 3 1 2 2 cmosp l=90n w=180n

mn1 3 1 0 0 cmosn l=90n w=180n

.control

run

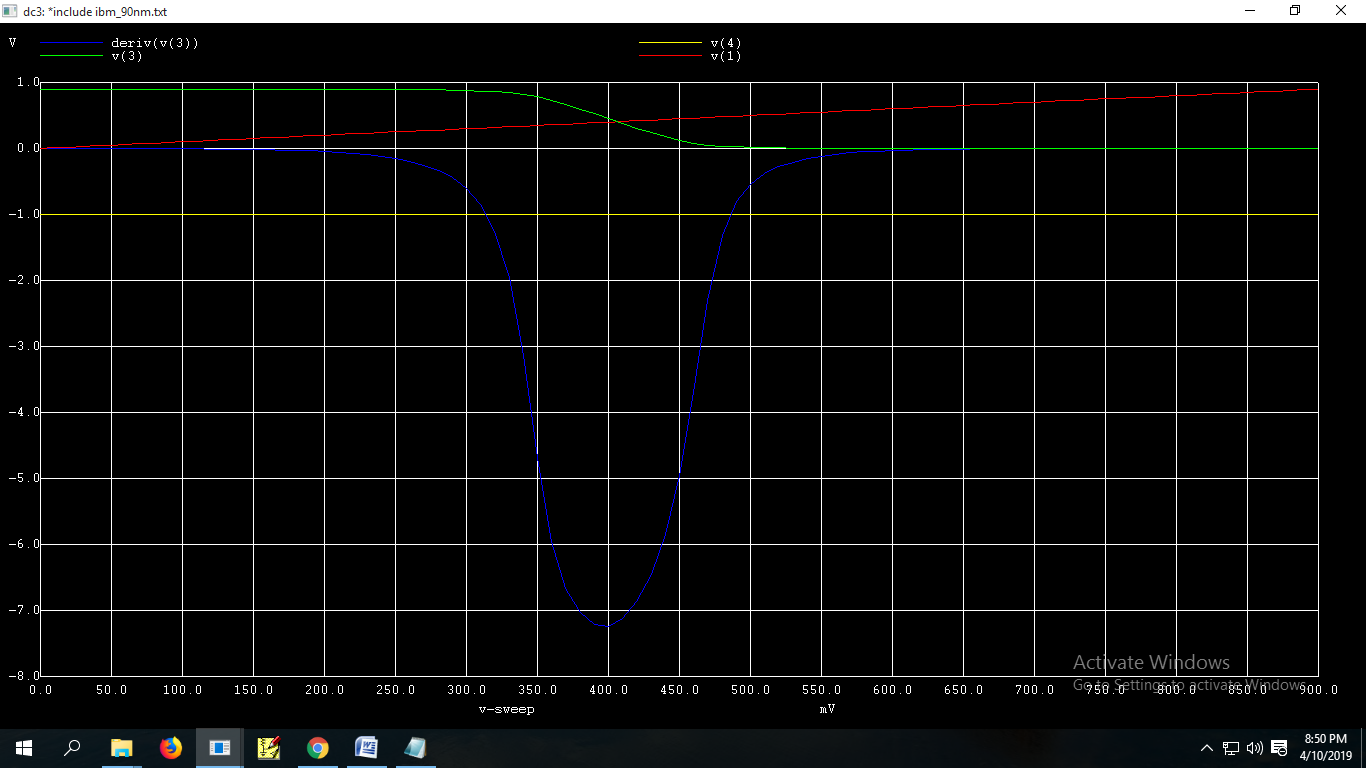
dc vin 0 0.9 10m

plot v(3) v(1) deriv(v(3)) v(4)

.endc

.end

**SCREENSHOTS:**



**Conclusion:** VOH = 0.9v, VOL =0v, VIH= 0.4862, VIL=0.3144

NMH=0.413, NML=0.3144

1. Plot VTC for CMOS inverter with varying VDD.

.include ibm\_90nm.txt

vdd 2 0 0.9

vin 1 0 0.9

vref 4 0 -1

mn 3 1 2 2 cmosp l=90n w=180n

mn1 3 1 0 0 cmosn l=90n w=180n

.control

run

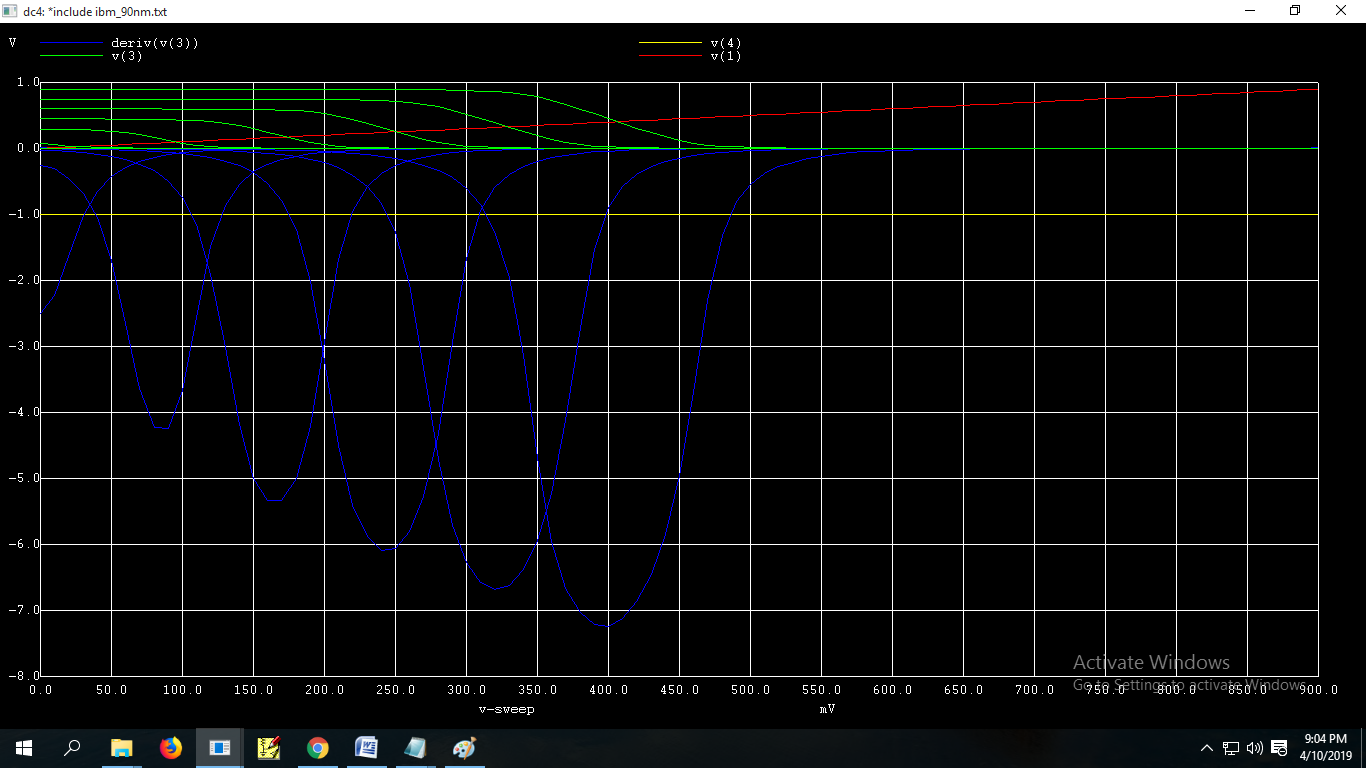
dc vin 0 0.9 10m vdd 0 0.9 0.15

plot v(3) v(1) deriv(v(3)) v(4)

.endc

.end

**SCREENSHOTS:**

****3) Plot VTC for CMOS inverter with varying device ratio.

.include ibm\_90nm.txt

vdd 2 0 0.9

vin 1 0 0.9

mn 3 1 2 2 cmosp l=90n w=90n

mn1 3 1 0 0 cmosn l=90n w=90n

mn2 4 1 2 2 cmosp l=90n w=180n

mn3 4 1 0 0 cmosn l=90n w=90n

mn4 5 1 2 2 cmosp l=90n w=90n

mn5 5 1 0 0 cmosn l=90n w=180n

mn6 6 1 2 2 cmosp l=90n w=360n

mn7 6 1 0 0 cmosn l=90n w=360n

.control

run

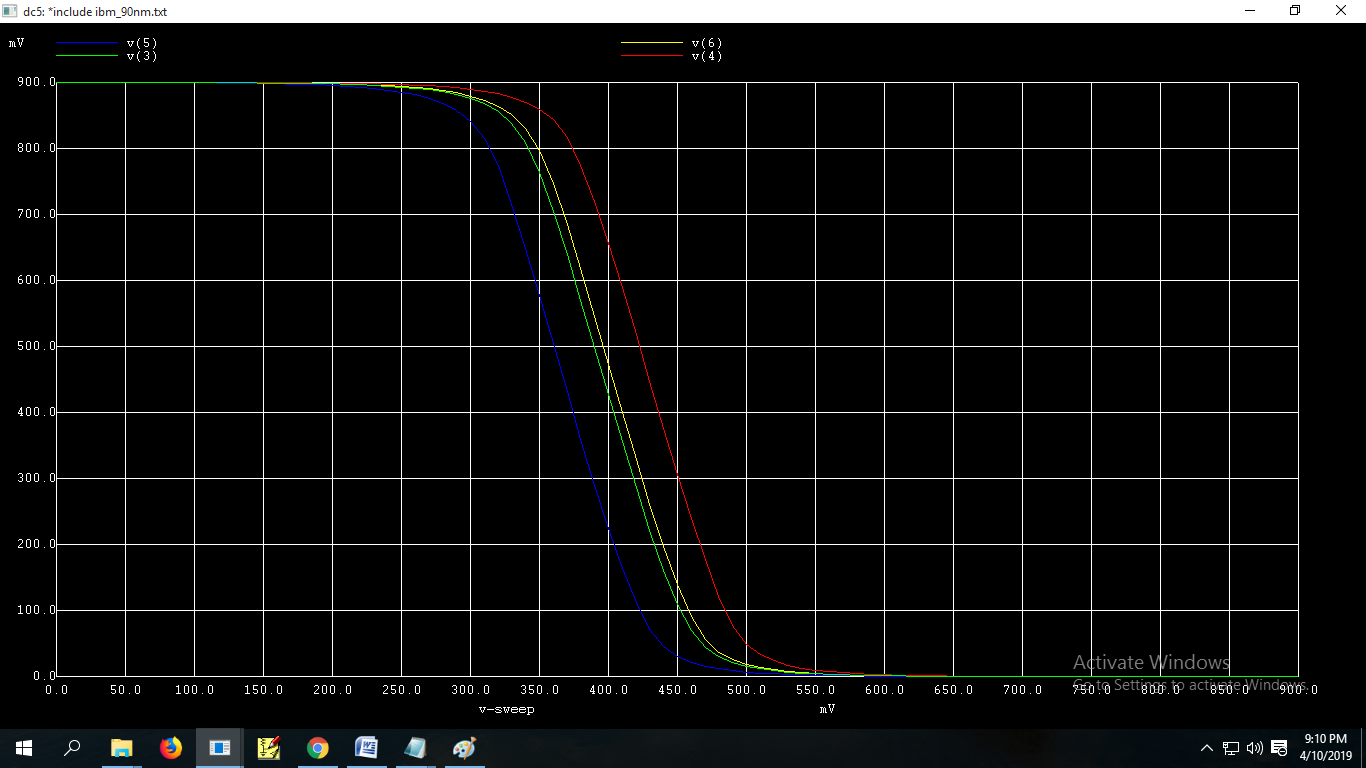
dc vin 0 0.9 10m

plot v(3) v(4) v(5) v(6)

.endc

.end

**SCREENSHOTS:**

****

**Conclusion:**  As we increases width of PMOS VTC shift towards right side

While increase in width of NMOS VTC shift towards left side

Same happen with Transaction Point.

4) Give pulse to inverter and find tphl , tplh, td.

.include ibm\_90nm.txt

vdd 2 0 0.9

vin 1 0 PULSE(0 0.9 0 10uS 10uS 40uS 100uS)

vref 4 0 0.45

vref1 5 0 0.09

vref2 6 0 0.81

c1 3 0 50pf

mn 3 1 2 2 cmosp l=90n w=180n

mn1 3 1 0 0 cmosn l=90n w=180n

.control

run

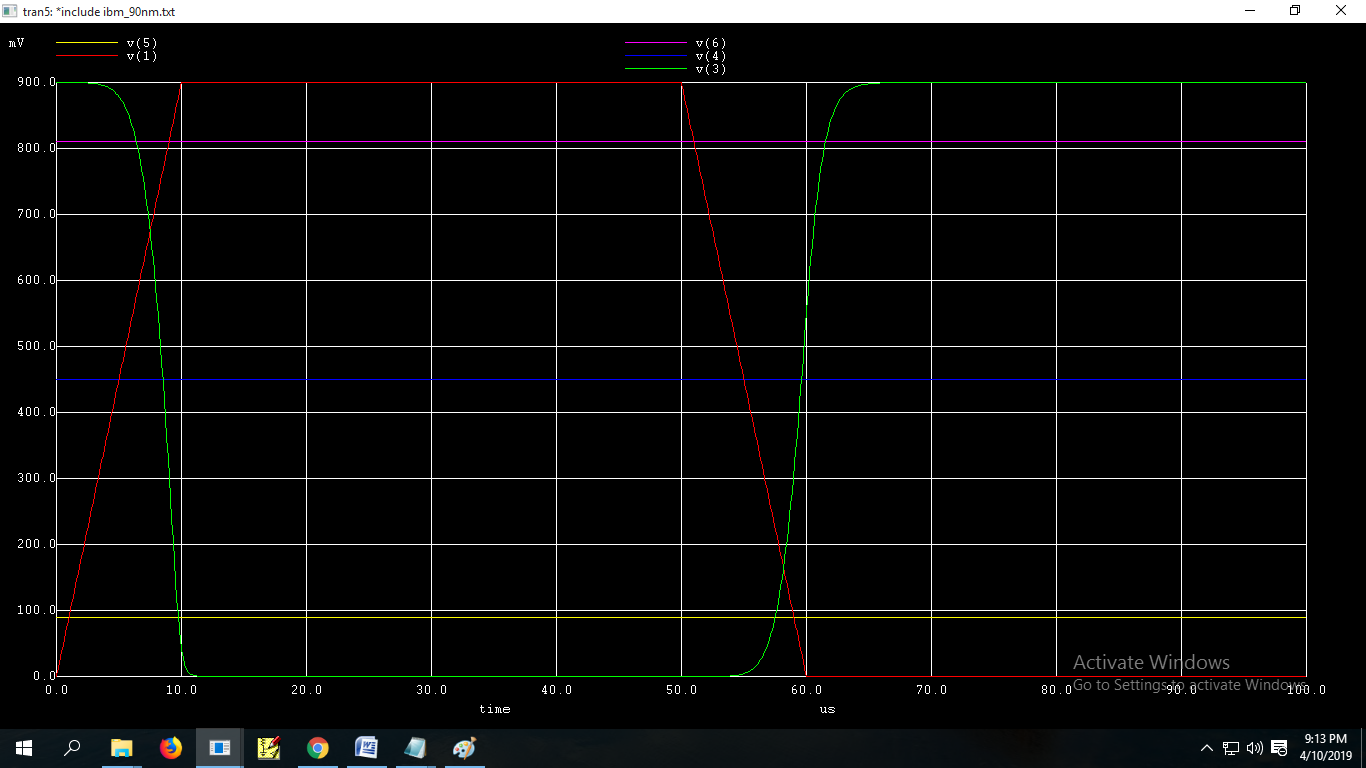
tran 100n 100u

plot v(3) v(1) v(4) v(5) v(6)

.endc

.end

**SCREENSHOTS:**



**Conclusion**: trise = 4.16 × , tfall= 3.456×

tplh = 3.42 × , tfall= 4.8×

Tp =

**Practical – 4**

**Aim:** Use NGSPICE to build a three stage and a eleven stage ring oscillator circuit in 90nm technology and compare its frequencies and time period.

1(a). 3 stage ring oscillator :

.include ibm\_90nm.txt

.subckt inv 1 3 2 0

c1 3 0 10pf

MN 3 1 0 0 cmosn l=90n w=180n

MN1 3 1 2 2 cmosp l=90n w=180n

.ends

vdd 2 0 2

xinv1 4 5 2 0 inv

xinv2 5 6 2 0 inv

xinv3 6 4 2 0 inv

.control

run

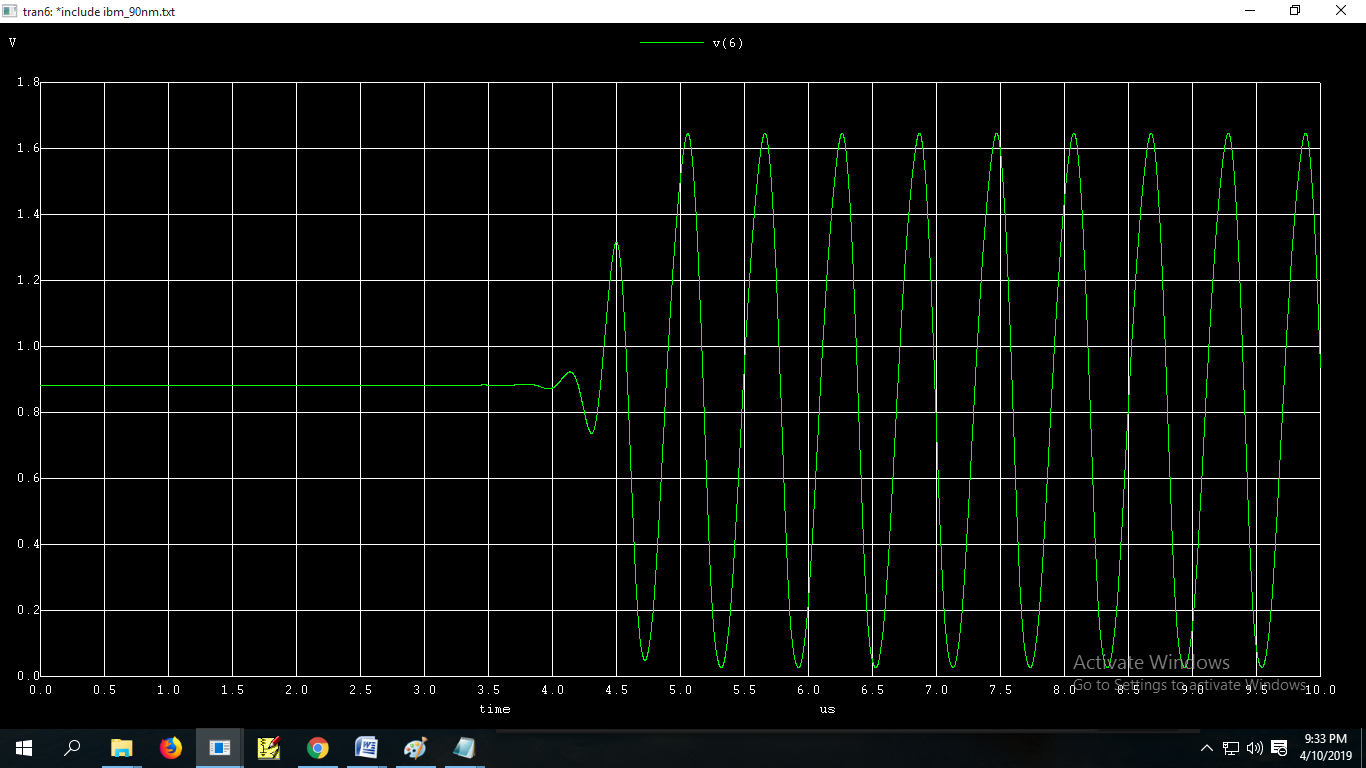
tran 1n 10u

plot v(6)

.endc

.end

**SCREENSHOTS:**



1(b). 3 stage ring oscillator with pulse:

.include ibm\_90nm.txt

vin 1 0 pulse(0 0.9 0 0.4us 0.4us 1us 2.8us)

vdd 2 0 0.9

c1 vout 0 1pf

c2 vout1 0 1pf

c3 vout2 0 1pf

vref1 ref 0 0.45

vref2 a 0 0.675

vref3 b 0 0.225

mn vout 1 0 0 cmosn l=90n w=180n

mn2 vout 1 2 2 cmosp l=90n w=180n

mn3 vout1 vout 0 0 cmosn l=90n w=180n

mn4 vout1 vout 2 2 cmosp l=90n w=180n

mn5 vout2 vout1 0 0 cmosn l=90n w=180n

mn6 vout2 vout1 2 2 cmosp l=90n w=180n

.control

run

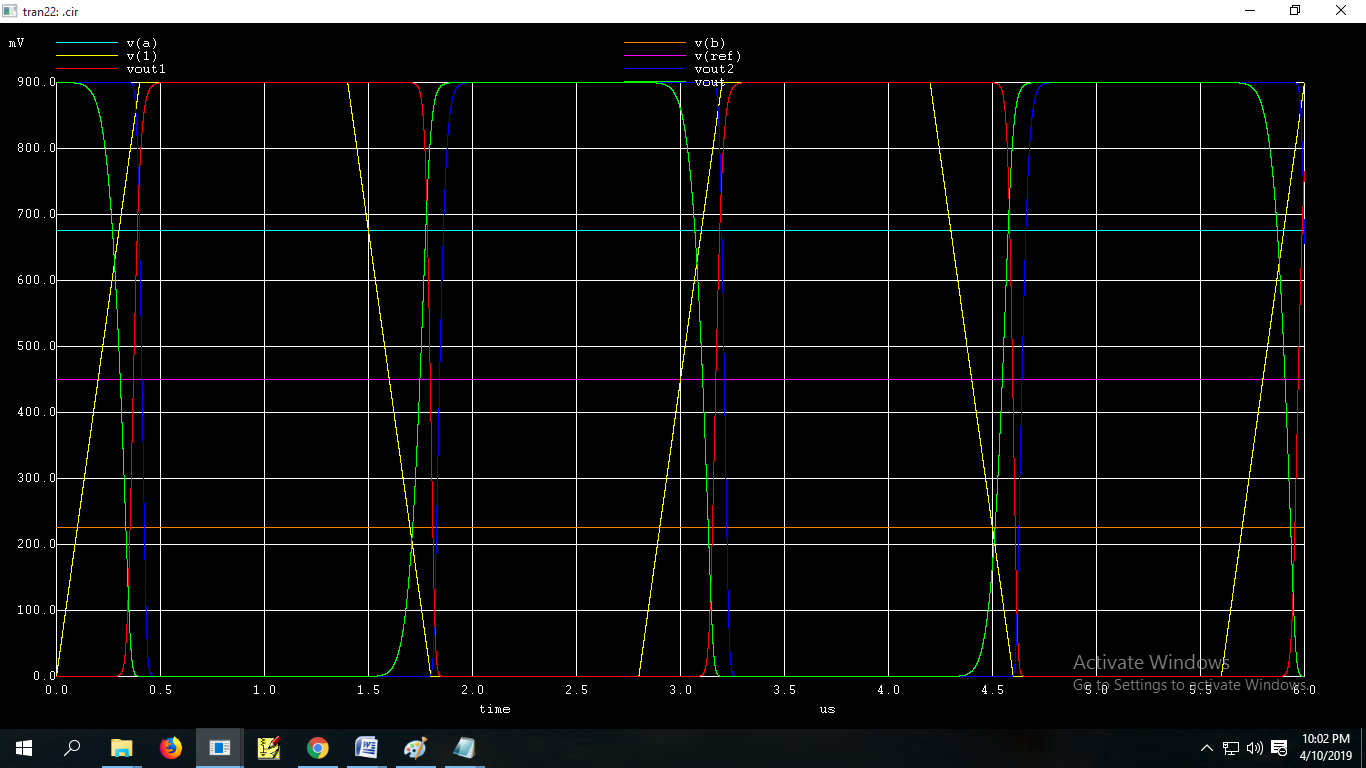
tran 0.1n 6u

plot vout vout1 vout2 v(1) v(ref) v(a) v(b)

.endc

.end

**SCREENSHOTS:**



1. 11 stage Oscillator:

.include ibm\_90nm.txt

.subckt inv 1 3 2 0

c1 3 0 10pf

MN 3 1 0 0 cmosn l=90n w=180n

MN1 3 1 2 2 cmosp l=90n w=180n

.ends

vdd 2 0 2

xinv1 4 5 2 0 inv

xinv2 5 6 2 0 inv

xinv3 6 7 2 0 inv

xinv4 7 8 2 0 inv

xinv5 8 9 2 0 inv

xinv6 9 10 2 0 inv

xinv7 10 11 2 0 inv

xinv8 11 12 2 0 inv

xinv9 12 13 2 0 inv

xinv10 13 14 2 0 inv

xinv11 14 4 2 0 inv

.control

run

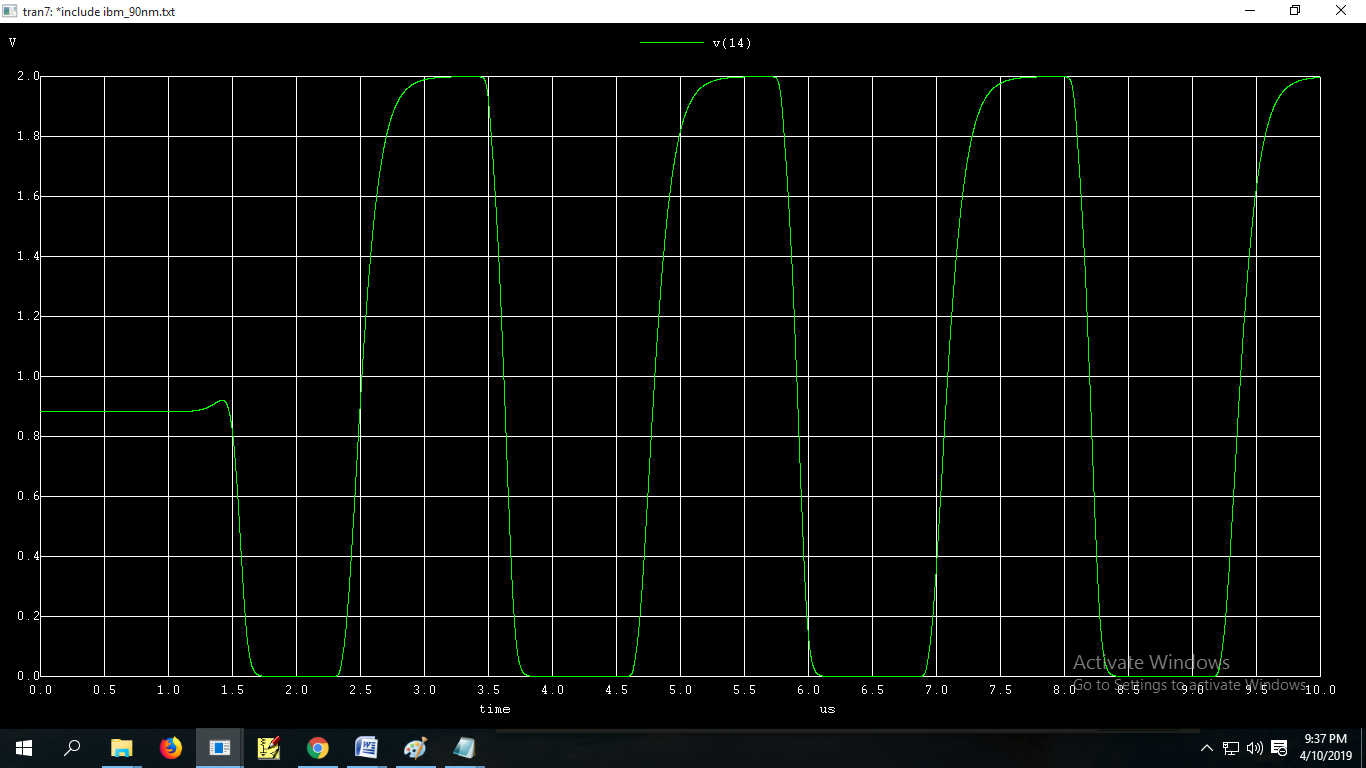
tran 1n 10u

plot v(14)

.endc

.end

**SCREENSHOTS:**



**Conclusion:**  frequency of 3 stage ring oscillator is 1.72Mhz.

And frequency of 11 stage ring oscillator is 0.438Mhz.

So as we increases number of stages propagation delay increases which results in reduction of frequency.

**Practical – 5**

**Aim:** Design an 6t SRAM and Sense amplifier and find out Cell Ratio and Pull up ratio of 6t SRAM cell

1(a) 6t SRAM (read operation)

.include ibm\_90nm.txt

c1 5 0 1pf

c2 4 0 1pf

vdd 2 0 0.9

v1 6 0 0.9

mn1 3 1 2 2 cmosp l=90n w=90n //qbar

mn2 3 1 0 0 cmosn l=90n w=360n

mn3 1 3 2 2 cmosp l=90n w=90n //q

mn4 1 3 0 0 cmosn l=90n w=90n

mn5 5 6 1 0 cmosn l=90n w=300n //bit

mn6 4 6 3 0 cmosn l=90n w=180n //bit bar

.ic v(5)=0.9 v(4)=0.9 v(1)=0 v(3)=0.9

.control

run

tran 1n 5u

plot v(1) v(3) v(4) v(5)

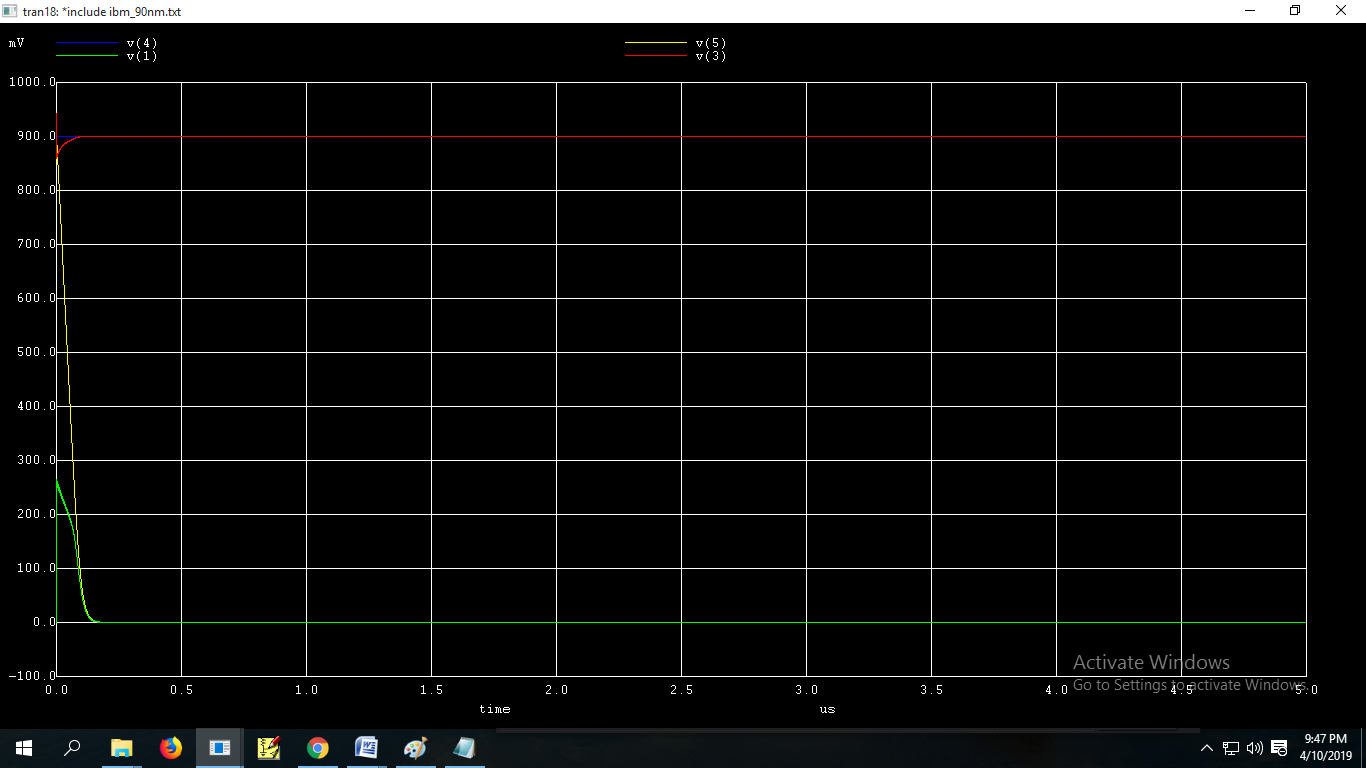
.endc

.end

\*\*for w/l of mn5 >320 condition fail for read

\*\* cell ratio must be > 0.28

**SCREENSHOTS:**



1(b) 6t SRAM (Write operation)

.include ibm\_90nm.txt

c1 5 0 1pf

c2 4 0 1pf

vdd 2 0 0.9

v1 6 0 0.9

mn1 3 1 2 2 cmosp l=90n w=1730n //qbar

mn2 3 1 0 0 cmosn l=90n w=360n

mn3 1 3 2 2 cmosp l=90n w=90n //q

mn4 1 3 0 0 cmosn l=90n w=360n

mn5 5 6 1 0 cmosn l=90n w=180n //bit

mn6 4 6 3 0 cmosn l=90n w=180n //bit bar

.ic v(5)=0.9 v(4)=0 v(1)=0 v(3)=0.9

.control

run

tran 1n 5u

plot v(1) v(3) v(4) v(5)

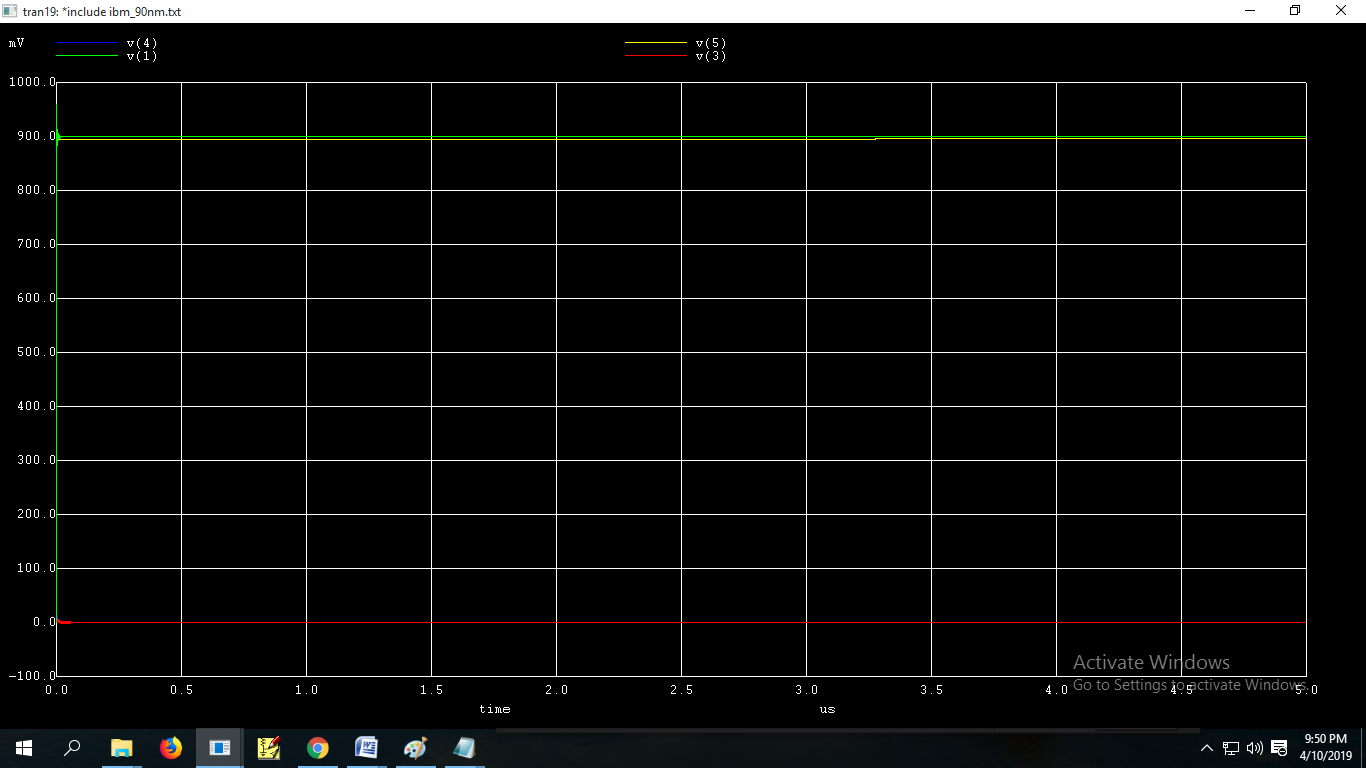
.endc

.end

\*\*for w/l of mn1>1730 condion fail for write

\*\*pull up ratio is < 9.61

**SCREENSHOTS:**



2 Sense Amplifier:

.include ibm\_90nm.txt

c1 5 0 1pf

c2 4 0 1pf

vdd 2 0 0.9

vdc 9 0 0.9

vdb 6 0 0.9

vde 7 0 0.9

//SRAM

mn1 3 1 2 2 cmosp l=90n w=90n //qbar

mn2 3 1 0 0 cmosn l=90n w=360n

mn3 1 3 2 2 cmosp l=90n w=90n //q

mn4 1 3 0 0 cmosn l=90n w=360n

mn5 5 6 1 0 cmosn l=90n w=180n //bit

mn6 4 6 3 0 cmosn l=90n w=180n //bit bar

//SENSE\_AMPLIFIER

mn7 5 4 9 9 cmosp l=90n w=90n //qbar

mn8 5 4 8 0 cmosn l=90n w=360n

mn9 4 5 9 9 cmosp l=90n w=90n //q

mn10 4 5 8 0 cmosn l=90n w=360n

mn11 8 7 0 0 cmosn l=90n w=180n //sense\_enable

.ic v(5)=0.9 v(4)=0.9 v(1)=0 v(3)=0.9

.control

run

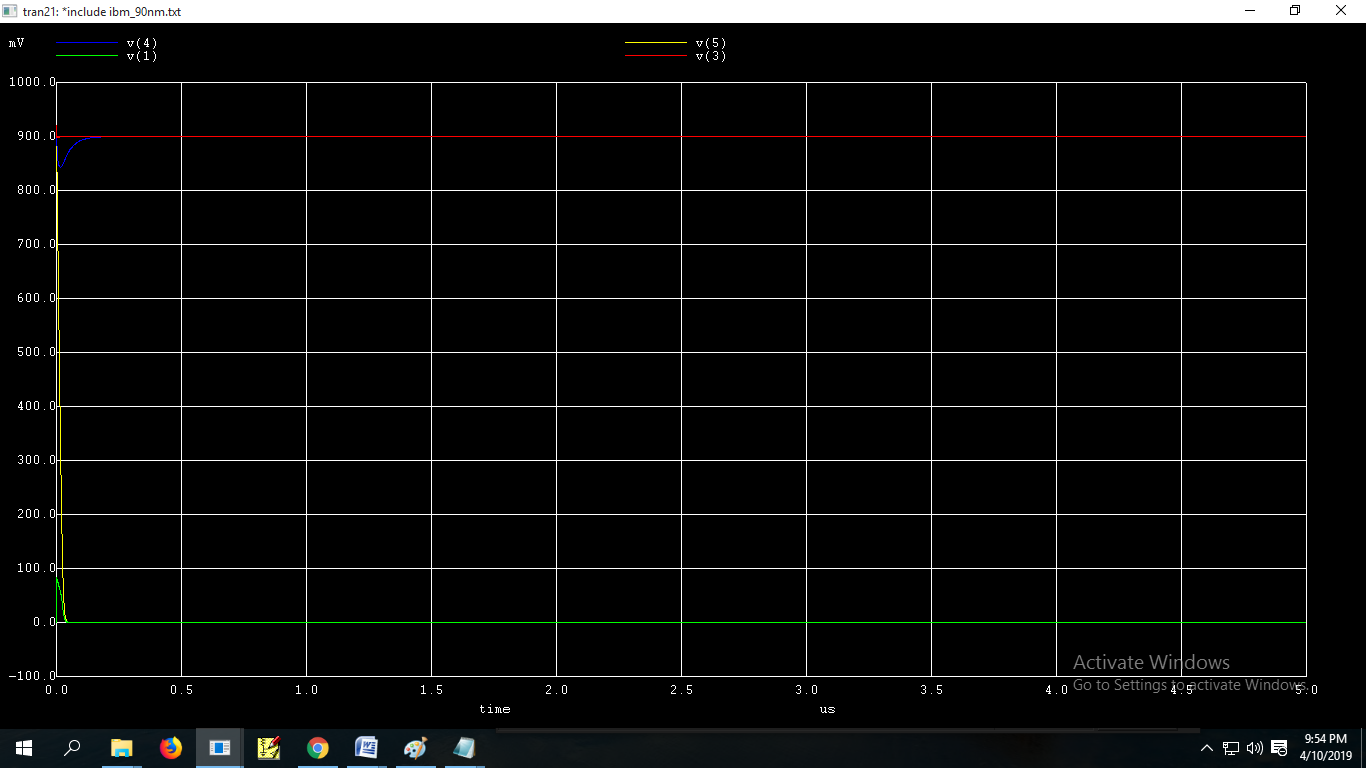
tran 1n 5u

plot v(1) v(3) v(4) v(5)

.endc

.end

**SCREENSHOTS:**



**Conclusion:**  for w/l of mn5 >320 condition fail for read. For proper read operation we have to maintain ratio of mn4 to mn5 should be greater than 0.28 which is also called as cell ratio.

cell ratio must be > 0.28

for w/l of mn1>1730 condion fail for write. . For proper write operation we have to maintain ratio of mn1 to mn6 should be less than 9.61 which is also called as pull up ratio.

pull up ratio is < 9.61